PLASMA DISPLAY PANEL AND METHOD OF FABRICATING THE SAME

[0001] This application claims the benefit of the Korean Patent Application No. P2003-26401 filed in Korea on April 25, 2003, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a plasma display panel, and more particularly to a plasma display panel that is adaptive for improving yield and mass productivity and a fabricating method thereof.

Description of the Related Art

[0003] A plasma display panel (hereinafter 'PDP') has light emission of phosphorus caused by ultraviolet rays of 147nm that is generated upon discharge of inert mixed gas such as He+Xe, Ne+Xe, He+Xe+Ne, thereby displaying a picture including characters or graphics. Such a PDP is easy to be made into a thin-film and large-dimension type of it. Moreover, the PDP provides a very improved picture quality owing to recent technical development.

[0004] Referring to FIG. 1, a discharge cell of a three-electrode

AC surface discharge type PDP includes a sustain electrode pair 4 formed on an upper substrate 16 and an address electrode 2 formed on a lower substrate 14.

[0005] Each of the sustain electrode pair 4 includes a transparent electrode 4A of indium tin oxide ITO and a metal bus electrode 4B formed at one side of the edge of the transparent electrode 4A. An upper dielectric layer 12 and a protective film 10 are deposited on the upper substrate 16 where the sustain electrode pair 4 has been formed. Wall charges generated upon plasma discharge are accumulated in the upper dielectric layer 12. The protective film 10 prevents the upper dielectric layer 12 and the sustain electrode pair 4 from being damaged due to sputtering generated upon plasma discharge, and in addition, it increases the emission efficiency of secondary electron. The protective film 10 is normally magnesium oxide MgO.

[0006] A lower dielectric layer 18 and barrier ribs 8 are formed on the lower substrate 14 where address electrode 2 has been formed, and a phosphorus 6 is formed on the surface of the lower dielectric layer 18 and the barrier ribs 8. The address electrode 2 is orthogonal to the sustain electrode pair 4. The barrier ribs 8 are formed along the address electrode 2 to prevent the ultraviolet ray and visible ray generated by discharge from leaking out to adjacent discharge cells. The phosphorus 6 is excited by the vacuum ultraviolet ray generated upon plasma discharge to generate any one of red, green or blue visible ray.

[0007] Inert mixed gas such as He+Xe, Ne+Xe, He+Xe+Ne is injected for discharge into a discharge space of the discharge cell provided

between the upper/lower substrate 16, 14 and the barrier ribs 8.

[0008] On the other hand, the lower substrate 14 where the address electrode 2 has been formed is joined with the upper substrate 16 where the sustain electrode pair 4Y, 4Z has been formed, as shown in FIG. 2, by a sealing layer 50.

[0009] FIGs. 3A to 3D are sectional diagrams representing a sealing process of PDP of prior art.

[0010] Firstly, the sustain electrode pair 4Y, 4Z and the upper dielectric layer 12 are formed on the upper substrate 16, as shown in FIG. 3A.

[0011] The sealing layer 50, as shown in FIG. 3B, is formed on the upper substrate 16 where the upper dielectric layer 12 has been formed. The sealing layer 50 is formed by spreading sealing-paste in use of a screen printing or a dispenser, wherein the sealing-paste is formed by mixing glass powder, solvent and binder together.

[0012] Subsequently, Under the environment of 200~300℃, the protective film 10 is formed on the upper substrate 16 in use of E-beam deposition or sputtering methods, as shown in FIG. 3.

[0013] Subsequently, the upper substrate 16 is aligned with the lower substrate 14 while the upper substrate 16 where the sealing layer 50 has been formed is pressed against and joined with the lower substrate 14. The aligned upper substrate 16 and lower substrate 14 are fired to remove a large amount of solvent and organic

material which are contained within the sealing layer 50, thereby joining the upper/lower substrate 16, 14, as shown in FIG. 3D.

[0014] However, after the protective film 10 is formed under the environment of 200~300, there occurs a crack in the area of the upper substrate 16 contacted with the sealing layer 50 due to the difference of thermal expansion coefficient between the upper substrate 16 and the sealing layer 50 in the course that it cools down to normal temperature. The difference of such thermal expansion coefficients generates partial thermal stress on a part where the upper substrate 16 is in contact with the sealing layer 50. There is generated a thermal stress which is relatively bigger in the upper substrate 16 than in the sealing layer 50, wherein the upper substrate 16 has relatively bigger thermal expansion coefficient than the sealing layer 50, and the thermal stress causes the crack to be generated in the upper substrate 16.

[0015] Accordingly, there is a problem that the yield and mass productivity of PDP is decreased.

SUMMARY OF THE INVENTION

[0016] Accordingly, it is an object of the present invention to provide a plasma display panel that is adaptive for improving yield and mass productivity and a fabricating method thereof.

[0017] In order to achieve these and other objects of the invention, a plasma display panel according to an aspect of the present invention includes a first substrate; a second substrate

facing the first substrate with a discharge space therebetween; a sealing layer located between the first substrate and the second substrate; and a buffer layer formed between the first substrate and the sealing layer to compensate the thermal stress of the first substrate and the sealing layer.

[0018] The buffer layer is composed of PbO of 45~55%, B2O3 of 10~20%, Al2O3 of 10~20% and SiO2 of 15~25%.

[0019] The thermal expansion coefficient of the buffer layer is different from the thermal expansion coefficient of the first substrate.

[0020] The thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the first substrate.

[0021] The thermal expansion coefficient of the buffer layer is different from the thermal expansion coefficient of the sealing layer.

[0022] The thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the sealing layer.

[0023] The thermal expansion coefficient of the first substrate is around $80X10^{-7}$~$95X10^{-7}$/℃.

[0024] The thermal expansion coefficient of the sealing layer is around $65X10^{-7}$~$80X10^{-7}$/℃.

[0025] The thermal expansion coefficient of the buffer layer is around $72X10^{-7}$~$86X10^{-7}$/℃.

[0026] The plasma display panel further includes a protective film formed on the first substrate where the buffer layer has been formed.

[0027] The plasma display panel further includes an upper dielectric layer formed on the first substrate; and a protective film formed on the upper dielectric layer.

[0028] The buffer layer is formed to be extended from the upper dielectric layer.

[0029] The buffer layer is separately formed of a different material from the upper dielectric layer.

[0030] The buffer layer is formed of the same material as the upper dielectric layer.

[0031] A fabricating method of a plasma display panel according to another aspect of the present invention includes the steps of: forming a buffer layer on a first substrate; and forming a sealing layer on the buffer layer.

[0032] The fabricating method further includes the steps of: providing a second substrate facing the first substrate where the sealing layer has been formed; and joining the first substrate with the second substrate.

[0033] The fabricating method further includes the steps of: forming an upper dielectric layer on the first substrate; and forming a protective film on the upper dielectric layer.

[0034] In the fabricating method, the buffer layer is composed of PbO of 45~55%, B_2O_3 of 10~20%, Al_2O_3 of 10~20% and SiO_2 of 15~25%.

[0035] In the fabricating method, the thermal expansion coefficient of the buffer layer is different from the thermal expansion coefficient of the first substrate.

[0036] In the fabricating method, the thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the first substrate.

[0037] In the fabricating method, the thermal expansion coefficient of the buffer layer is different from the thermal expansion coefficient of the sealing layer.

[0038] In the fabricating method, the thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the sealing layer.

[0039] In the fabricating method, the thermal expansion coefficient of the first substrate is around $80X10^{-7}$~$95X10^{-7}$/℃.

[0040] In the fabricating method, the thermal expansion coefficient of the sealing layer is around $65X10^{-7}$~$80X10^{-7}$/℃.

[0041] In the fabricating method, the thermal expansion coefficient of the buffer layer is around $72X10^{-7}$~$86X10^{-7}$/℃.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

[0043] FIG. 1 is a perspective view representing a discharge cell structure of a 3-electrode AC type plasma display panel of prior art;

[0044] FIG. 2 is a sectional diagram representing a discharge cell structure of the plasma display panel, as shown in FIG. 1;

[0045] FIGs. 3A to 3D are sectional diagrams representing a sealing process of the plasma display panel of prior art;

[0046] FIG. 4 is a sectional diagram representing a discharge cell structure of a plasma display panel according to a first embodiment of the present invention;

[0047] FIG. 5 is a diagram representing that an upper dielectric layer of the plasma display panel according to the first embodiment of the present invention is double-layered;

[0048] FIG. 6A to 6D are sectional diagrams representing a

sealing process of the plasma display panel according to the first embodiment of the present invention;

[0049] FIG. 7 is a sectional diagram representing a discharge cell structure of a plasma display panel according to a second embodiment of the present invention;

[0050] FIG. 8 is a diagram representing that a buffer layer of the plasma display panel according to the second embodiment of the present invention is double-layered;

[0051] FIG. 9A to 9D are sectional diagrams representing a sealing process of the plasma display panel according to the second embodiment of the present invention;

[0052] FIG. 10 is a sectional diagram representing a discharge cell structure of a plasma display panel according to a third embodiment of the present invention;

[0053] FIG. 11 is a sectional diagram representing that a buffer layer of the plasma display panel according to the third embodiment of the present invention is lower in height than an upper dielectric layer; and

[0054] FIG. 12A to 12C are sectional diagrams representing a sealing process of the plasma display panel according to the third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0055] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0056] With reference to FIGs. 4 to 12C, embodiments of the present invention will be explained as follows.

[0057] FIG. 4 is a sectional diagram representing a PDP according to a first embodiment of the present invention.

[0058] Referring to FIG. 4, a discharge cell of a 3-electrode AC surface discharge type PDP includes a sustain electrode pair 104Y, 104Z formed on an upper substrate 116, and an address electrode 102 formed on a lower substrate 114. Herein, a sealing layer 150 joins the upper substrate 116 with the lower substrate 114.

[0059] Each of the sustain electrode pair 104Y, 104Z includes a transparent electrode 104A of indium tin oxide ITO and a metal bus electrode 104B formed at one side of the edge of the transparent electrode 104A. An upper dielectric layer 112 and a protective film 110 are deposited on the upper substrate 116 where the sustain electrode pair 104Y, 104Z have been formed. The upper dielectric layer 112 is extended to the sealing area of the upper substrate 116, so as to be in contact with the sealing layer. Also, wall charges generated upon plasma discharge are accumulated in the upper dielectric layer 112. The protective film 110 prevents the upper dielectric layer 112 and the sustain electrode pair 104 from being damaged due to sputtering generated upon plasma discharge, and in addition, it increases the emission efficiency of secondary electron.

The protective film 110 is normally magnesium oxide MgO.

[0060] A lower dielectric layer 118 and barrier ribs 108 are formed on the lower substrate 114 where the address electrode 102 has been formed, and a phosphorus 106 is formed on the surface of the lower dielectric layer 118 and the barrier ribs 108. The address electrode 102 is orthogonal to the sustain electrode pair 104Y, 104Z. The barrier ribs 108 are formed along the address electrode 102 to prevent the ultraviolet ray and visible ray generated by discharge from leaking out to adjacent discharge cells. The phosphorus 106 is excited by the vacuum ultraviolet ray generated upon plasma discharge to generate any one of red, green or blue visible ray.

[0061] Inert mixed gas such as He+Xe, Ne+Xe, He+Xe+Ne is injected for discharge into a discharge space of the discharge cell provided between the upper/lower substrate 116, 114 and the barrier ribs 108.

[0062] On the other hand, the upper dielectric layer 112 according to the first embodiment of the present invention is formed between the upper substrate 116 and the sealing layer 150 to alleviate the difference of thermal stress between them. To explain this in detail, the upper substrate 116 has a first thermal expansion coefficient, the sealing layer 150 has a second thermal expansion coefficient relatively lower than the first thermal expansion coefficient, and the upper dielectric layer 112 has a third thermal expansion coefficient between the first and second thermal expansion coefficients. For example, the thermal expansion coefficient of the upper substrate 116 is $80X10^{-7} \sim 95X10^{-7}$ /℃, the thermal expansion

coefficient of the sealing layer 150 is $65X10^{-7} \sim 80X10^{-7}$ /℃, and the thermal expansion coefficient of the upper dielectric layer 112 is $72X10^{-7} \sim 86X10^{-7}$ /℃.

[0063] Accordingly, the upper dielectric layer 112 located between the upper substrate 116 and the sealing layer 150 disperses the thermal stress caused by the difference of thermal expansion coefficient between the upper substrate 116 and the sealing layer 150 in the course that the upper substrate 116 cools down to normal temperature after the protective film 110 is formed under the environment of 200~300℃. Since the thermal stress is dispersed by the upper dielectric layer 112, it is possible to prevent a crack from occurring in the upper substrate 116 that overlaps with the sealing layer 150 while having the upper dielectric layer 112 therebetween. Herein, the composition and content of the upper dielectric layer 112 is as follows.

[Table 1]

Composition	PbO	B_2O_3	Al_2O_3	SiO_2
Content	45~55%	10~20%	10~20%	15~20%

[0064] On the other hand, as shown in FIG. 5, the upper dielectric layer 112 of the PDP according to the first embodiment of the present invention can be formed to be a double layer, and the sealing layer 150 can be formed on a first lower dielectric layer 112A that has been formed on the substrate 116.

[0065] FIGs. 6A to 6D are sectional diagrams representing a sealing process of the PDP according to the embodiment of the present

invention.

[0066] Firstly, an upper dielectric layer material is spread on the upper substrate 116 on which the sustain electrode pair 104Y, 104Z have been formed, thereby forming the upper dielectric layer 112 on the front surface of the upper substrate 116, as shown in FIG. 6A. The sealing layer 150 is formed on the upper substrate 116 where the upper dielectric layer 112 has been formed, as shown in FIG. 6B. The sealing layer 150 is formed by spreading a paste in use of screen printing or dispenser, wherein the paste is formed by mixing glass powder, solvent and binder together.

[0067] Subsequently, as shown in FIG. 6C, a protective film 110 is formed on the upper substrate 116, on which the sealing layer 150 has been formed, by using E-beam deposition or sputtering method under the environment of 200~300℃.

[0068] Subsequently, the upper substrate 116 where the sealing layer 150 has been formed is aligned with the lower substrate 114. The aligned upper substrate 116 and the lower substrate 114 are fired to remove a large amount of solvent and organic material which is contained within the sealing layer, thereby joining the upper/lower substrate 116, 114, as shown in FIG. 6D.

[0069] FIG. 7 is a sectional diagram representing a PDP according to a second embodiment of the present invention.

[0070] Referring to FIG. 7, the PDP according to the second embodiment of the present invention, when compared with the PDP shown in FIG. 4, has the same components except that it further

includes a buffer layer 211 between the upper substrate 216 and the upper dielectric layer 212, so there will be no detail explanation for the same components as shown in FIG. 4.

[0071] The buffer layer 211 is formed to be in contact with the sealing layer 250 at the lower part of the upper dielectric layer 212 and to have its thickness of 5~50μm on the entire surface of the upper substrate 216.

[0072] The buffer layer 211 is made of a material that has its thermal expansion coefficient between the thermal expansion coefficient of the upper substrate 216 and the thermal expansion coefficient of the sealing layer 250. For example, the thermal expansion coefficient of the upper substrate 216 is $80X10^{-7}$ ~ $95X10^{-7}$ /℃, the thermal expansion coefficient of the sealing layer 250 is $65X10^{-7}$ ~ $80X10^{-7}$ /℃, and the thermal expansion coefficient of the buffer layer 211 is $72X10^{-7}$ ~ $86X10^{-7}$ /℃. The material included in the buffer layer 211 is the same material as in the upper dielectric layer 216.

[0073] Accordingly, the area of the buffer layer 211 that is in contact with the sealing layer 250 disperses the thermal stress caused by the difference of thermal expansion coefficient between the upper substrate 216 and the sealing layer 250. Since the thermal stress is dispersed by the buffer layer 211, it is possible to prevent a crack from occurring in the upper substrate 216. Herein, the composition and content of the buffer layer 211 is as in table 2, and it is the same as the composition and content of the upper dielectric layer 212.

[Table 2]

Composition	PbO	B_2O_3	Al_2O_3	SiO_2
Content	45~55%	10~20%	10~20%	15~25%

[0074] On the other hand, as shown in FIG. 8, the buffer layer 211 of the PDP according to the second embodiment of the present invention can be formed to be a double layer of first and second buffer layers 211A, 211B, and the buffer layer 211 can be formed in the first buffer layer 211A so that it can have lower height than the buffer layer 211 of FIG 7.

[0075] FIGs. 9A to 9D are sectional diagrams representing a sealing process of the PDP according to the embodiment of the present invention.

[0076] Firstly, the buffer layer 211 is formed on the front surface of the upper substrate 216 where the sustain electrode pair 204Y, 204Z have been formed, as shown in FIG. 9A. The upper dielectric layer 212 is formed in a display area on the buffer layer 211 by spreading a dielectric layer material on an area except for the sealing area of the upper substrate 216 where the buffer layer 211 has been formed. The sealing layer 250 is formed on the upper substrate 216 where the upper dielectric layer 212 has been formed, as shown in FIG. 9B. The sealing layer 250 is formed by spreading a sealing material paste in use of screen printing or dispenser, wherein the sealing material paste is formed by mixing glass powder, solvent and binder together.

[0077] Subsequently, as shown in FIG. 9C, a protective film

210 is formed on the upper substrate 216, on which the sealing layer 250 has been formed, by using E-beam deposition or sputtering method under the environment of 200~300℃.

[0078] Subsequently, the upper substrate 216 where the sealing layer 250 has been formed is aligned with the lower substrate 214. The aligned upper substrate 216 and the lower substrate 214 are fired to remove a large amount of solvent and organic material which is contained within the sealing layer, thereby joining the upper/lower substrate 216, 214, as shown in FIG. 9D.

[0079] FIG. 10 is a sectional diagram representing a PDP according to a third embodiment of the present invention.

[0080] Referring to FIG. 10, the PDP according to the third embodiment of the present invention, when compared with the PDP shown in FIG. 4, has the same components except that it further includes a buffer layer 311 between the upper substrate 316 and the sealing layer 350, so there will be no detail explanation for the same components as shown in FIG. 4.

[0081] The buffer layer 311 is formed on the upper substrate 316 to be in contact with the sealing layer 350 and to have its thickness of 5~50μm only at the area where it overlaps with the buffer layer 311. Herein, the buffer layer 311 might be formed to have lower height than the upper dielectric layer 311, as shown in FIG. 11.

[0082] The buffer layer 311 is made of a material that has its thermal expansion coefficient between the thermal expansion

coefficient of the upper substrate 316 and the thermal expansion coefficient of the sealing layer 350. For example, the thermal expansion coefficient of the upper substrate 316 is $80X10^{-7} \sim 95X10^{-7}$ /℃, the thermal expansion coefficient of the sealing layer 350 is $65X10^{-7} \sim 80X10^{-7}$ /℃, and the thermal expansion coefficient of the buffer layer 311 is $72X10^{-7} \sim 86X10^{-7}$ /℃. The material included in the buffer layer 311 is the same material as in the upper dielectric layer 316.

[0083] Accordingly, the area of the buffer layer 311 that is in contact with the sealing layer 350 disperses the thermal stress caused by the difference of thermal expansion coefficient between the upper substrate 316 and the sealing layer 350. Since the thermal stress is dispersed by the buffer layer 311, it is possible to prevent a crack from occurring in the upper substrate 316. Herein, the composition and content of the buffer layer 311 is as in table 3, and it is the same as the composition and content of the upper dielectric layer 312.

[Table 3]

Composition	PbO	B_2O_3	Al_2O_3	SiO_2
Content	45~55%	10~20%	10~20%	15~25%

[0084] FIGs. 12A to 12D are sectional diagrams representing a sealing process of the PDP according to the embodiment of the present invention.

[0085] The buffer layer 311 is formed at an area, which is to be described later, that the sealing layer 350 overlaps with the

upper substrate 316, as shown in FIG. 12, by spreading a buffer layer material on the upper substrate 316 where the sustain electrode pair 304Y, 304Z have been formed, as shown in FIG. 12A. Then, the upper dielectric layer 312 is formed by spreading a dielectric layer material on the upper substrate 316 except for an area where the buffer layer 311 has been formed. The sealing layer 350 is formed on the upper substrate 316 where the upper dielectric layer 312 has been formed, as shown in FIG. 12B. The sealing layer 350 is formed by spreading a paste in use of screen printing or dispenser, wherein the paste is formed by mixing glass powder, solvent and binder together.

[0086] Subsequently, a protective film 310 is formed on the upper substrate 316, on which the sealing layer 350 has been formed, by using E-beam deposition or sputtering method under the environment of 200~300℃. Subsequently, the upper substrate 316 where the sealing layer 350 has been formed is aligned with the lower substrate 314. The aligned upper substrate 316 and the lower substrate 314 are fired to remove a large amount of solvent and organic material which is contained within the sealing layer, thereby joining the upper/lower substrate 316, 314, as shown in FIG. 12C.

[0087] As described above, a plasma display panel and a fabricating method thereof according to the present invention extends the dielectric layer or forms the buffer layer between the upper substrate and the sealing layer, thereby dispersing the partial thermal stress generated upon heating or cooling due to the difference of thermal expansion coefficient between the upper substrate and the sealing layer, so that the crack on the upper substrate can be prevented.

[0088] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.